

**SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF**

Patent number: JP63316476  
Publication date: 1988-12-23  
Inventor: HOSAKA TAKASHI  
Applicant: SEIKO INSTR & ELECTRONICS LTD  
Classification:  
- international: H01L29/78  
- european:  
Application number: JP19870152236 19870618  
Priority number(s):

Also published as:  
US4954867 (A1)

[View INPADOC patent family](#)

**Abstract of JP63316476**

**PURPOSE:** To prevent gate electrode/wiring from being deteriorated due to heat treatment, by covering upper and side planes of the gate electrode/wiring with a silicon oxynitride film.

**CONSTITUTION:** A gate insulating film 2 is formed on a surface of a semiconductor, and a high-melting point metallic film 3 made of molybdenum or tungsten or the like is formed on the film 2, and a silicon oxynitride film 4 is produced by a CVD method. Photolithography or the like is used to perform selective etching of the oxynitride film 4 and the high-melting-point metallic film 3 serially so that gate electrode/wiring 3 of desired shape is formed. Next ion implantation for LDD (lightly Doped Drain) formation is performed to form source/ drain 8 of low concentration. A silicon oxynitride film 6 is formed again and the whole surface of the semiconductor is provided with much anisotropic etching so that side and upper planes of the high-melting-point metallic film and the wiring 3 are covered with the oxynitride film. Hence, the gate electrode/ wiring can be prevented from being deteriorated in its characteristics.

**BEST AVAILABLE COPY**